CLAIMS

1. A method for time multiplexing signals comprising:

merging a set of nets carrying the signals into a shared interconnect portion;

altering a netlist based on the merging; and

placing a design represented by the altered netlist.

2. A method of time multiplexing signals on interconnect in a programmable logic device, the method comprising:

merging the nets into a shared interconnect portion;

altering the design based on the merging;

placing the altered design; and

routing the altered design.

3. An integrated circuit comprising:

a set of configurable logic blocks comprising multiple signal sources; and

a time multiplexing signal generator controlling which of the multiple signal sources provides its signal to a corresponding signal destination.

4. The integrated circuit of Claim 3, wherein the multiple signal sources are located in one configurable logic block.

5. The integrated circuit of Claim 3, wherein the multiple signal sources generate critical signals.

6. The integrated circuit of Claim 3, wherein the time multiplexing signal generator includes a counter.